

## ABSTRACT OF THE DISCLOSURE

A streamlined cache coherency protocol system and method for a multiple processor single chip device. There are three primary memory unit (e.g., a cache line) states ( modified, shared, and invalid) and three intermediate memory unit pending states. The pending states are used by the present invention to prevent race conditions that may develop during the completion of a transaction. The pending states "lock out" the memory unit (e.g., prevent access by other agents to a cache line) whose state is in transition between two primary states, thus ensuring coherency protocol correctness. Transitions between states are governed by a series of request and reply or acknowledgment messages. The memory unit is placed in a pending state while appropriate measures are taken to ensure access takes place at an appropriate time. For example, a modification occurs only when other agents can not access the particular memory unit (e.g., a cache line).